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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MEICHUN HSU and QIMING CHEN

Appeal 2016-006550
Application 13/562,691[1]
Technology Center 2100

Before JOSEPH L. DIXON, JOYCE CRAIG, and
MATTHEW J. McNEILL, *Administrative Patent Judges*.

CRAIG, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Non-Final Rejection of claims 1–15, which constitute all of the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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[1] According to Appellants, the real party in interest is Hewlett-Packard Development Company, LP. App. Br. 1.

INVENTION

Appellants' application relates to queue and operator instance threads to losslessly process online input stream events. Abstract. Claim 1 is illustrative of the appealed subject matter and reads as follows:

> 1. An apparatus comprising:
>
> a processor;
>
> a computer-readable data storage medium;
>
> a queue implemented by the processor at the computer-readable data storage medium to enqueue an online input stream of events arriving at the queue in real-time;
>
> an operator instance implemented by the processor and having one or more threads to losslessly dequeue and process the events from the queue, and to output processing results of the events in a common output stream; and
>
> a control mechanism implemented by the processor to dynamically instantiate and destantiate the one or more threads to maintain an optimal number of the one or more threads while ensuring that none of the events of the online input stream are dropped.

REJECTIONS

Claims 1, 4, 5, 7–9, 12, and 13 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Pandey et al. (US 2011/0016123 A1; published Jan. 20, 2011) ("Pandey") and Andrade et al. (US 2011/0041132 A1; published Feb. 17, 2011) ("Andrade").

Claim 2 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Pandey, Andrade, and Porter et al. (US 7,321,939 B1; issued Jan. 22, 2008) ("Porter").

Claims 3, 10, and 14 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Pandey, Andrade, and Robison et al. (US 2003/0115168 A1; published June 19, 2003) ("Robison").

Claims 6 and 15 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Pandey, Andrade, and Welsh, "An Architecture for Highly Concurrent, Well-Conditioned Internet Services," dissertation, U.C. Berkeley (2002) ("Welsh").

Claim 11 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Pandey, Andrade, Robison, and Welsh.

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' contentions that the Examiner has erred. We disagree with Appellants' contentions. Except as noted below, we adopt as our own: (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken and (2) the reasons set forth by the Examiner in the Examiner's Answer in response to Appellants' Appeal Brief. We concur with the conclusions reached by the Examiner. We highlight the following additional points.

In rejecting claim 1, the Examiner found that Pandey teaches or suggests all of the recited limitations, except "a control mechanism implemented by the processor to dynamically instantiate and destantiate the one or more threads to maintain an optimal number of the one or more threads while ensuring that none of the events of the online input stream are dropped," for which the Examiner relied on Andrade. Non-Final Act. 2–4.

Appellants contend the Examiner erred because the cited portions of Pandey do not teach or suggest adapter threads that output processing results of events in a common output stream, as claim 1 requires. App. Br. 4. Appellants argue that adapter threads 129 of Pandey output plural "event streams." *Id.* (citing Pandey Fig. 1B, ¶¶ 56, 61).

Appellants' arguments do not persuade us of Examiner error. The Examiner found that Pandey teaches or suggests the recited processing results in a common output stream because the adapter threads read event data streams from the queues and format them to a format (Event Bean) that is common to all threads. Ans. 21–22. In the Reply Brief, Appellants argue that "the Examiner's contention is not correct" and "Pandey's 'desired Event Bean format' cannot be the same as the claimed 'common output stream.'" Reply Br. 3. Appellants' arguments are not commensurate in scope with the Examiner's findings. The Examiner did not equate Pandey's Event Bean format with the recited "common output stream," as Appellants contend. Rather, the Examiner found that Pandey's teaching that data formatted in the Event Bean format is common to each and every adapter thread teaches or suggests the recited "common output stream." *See* Ans. 21–22. Appellants offer insufficient persuasive argument or objective evidence to rebut the Examiner's findings. In particular, Appellants do not contend that the Examiner's interpretation of the claim term "common output stream" is overly broad, unreasonable, or inconsistent with Appellants' Specification.

Appellants next contend the cited portions of Pandey do not teach or suggest the limitation "an operator instance implemented by the processor and having one or more threads," recited in claim 1. App. Br. 5. Appellants argue that, in Pandey, "receiver 115 does not have the adapter threads 129"

and "a different component, a concurrent adapter 119, has the adapter threads 129." *Id.* (citing Pandey Fig. 1B).

Appellants' arguments are unpersuasive. We agree with the Examiner that the plain language of claim 1 does not require that the threads be inside or part of the operator instance. *See* Ans. 20. Claim 1 requires an operator instance "having" one or more threads. App. Br. 7. In support of their argument that the recited threads must be inside the operator instance, Appellants point to paragraph 24 of the Specification, which describes in pertinent part that "[t]he threads 106 are thus inside the same execution framework of the operator instance 104 . . . ." Reply Br. 2. Appellants, however, do not persuade us that threads "inside the same execution framework of an operator instance" means that the threads must be inside the operator instance. Moreover, paragraph 24 describes Figure 1, which the Specification describes as "an example system . . . ." Spec. ¶ 24. Although claims are interpreted in light of the Specification, limitations from the Specification are not read into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

For these reasons, we are not persuaded that the Examiner erred in finding that the combination of Pandey and Andrade teaches or suggests the limitations of claim 1.

Accordingly, we sustain the Examiner's 35 U.S.C. § 103(a) rejection of independent claim 1, as well as the 35 U.S.C. § 103(a) rejection of independent claims 8 and 13, which Appellants argue are patentable for similar reasons. App. Br. 4.[2] We also sustain the Examiner's rejection of

[2] Appellants erroneously identify claim 9 instead of claim 8, but properly reference claim 8 earlier in the same paragraph. *See* App. Br. 4.

dependent claims 2–7, 9–12, 14, and 15, for which Appellants make no separate arguments for patentability. *Id.* at 6.

DECISION

We affirm the decision of the Examiner rejecting claims 1–15.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED